UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,993	10/08/2003	Shinobu Isobe	5328-15	8976

27799 7590 12/29/2005

COHEN, PONTANI, LIEBERMAN & PAVANE
551 FIFTH AVENUE
SUITE 1210
NEW YORK, NY 10176

EXAMINER	
KIK, PHALLAKA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/681,993	ISOBE, SHINOBU	
	Examiner	Art Unit	
	Phallaka Kik	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2005 and 08 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) *3,4,6 and 7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/8/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to the Election filed on 12/8/2005, Application and IDS filed on 10/8/2003. Claims 1-7 are pending, wherein claims 3-4,6-7 are withdrawn from consideration, as being directed to non-elected inventions without traverse.

Election/Restrictions

2. Applicant's election without traverse of group I invention, claims 1-2,5 in the reply filed on 12/8/2005 is acknowledged.

3. **Claims 3-4,6-7** are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected inventions, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 12/8/2005.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

5. Figures 6, 7A, 7B, 8A, 8B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated (see Applicant's specification, page 7, line 25 to page 8, line 5; page 1, line 10 to page 3, line 12). See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the

examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

6. **Claims 1-2,5** are objected to because of the following informalities:

As per **claim 1**, "the measurement" (line 6) should be --each-- for proper antecedent basis; "which" (line 7) should be --said wiring line-- to clearly that the "wiring line" and not the "circuit block" is formed in any layer of the semiconductor device.

As per **claim 2**, "which the" (line 3) should be --which each-- for proper antecedent basis. The claim is also objected to for incorporating the above errors into the claim by claim dependency.

As per **claim 5**, "the measurement" (line 6) should be --each-- for proper antecedent basis; "which" (line 7) should be --said wiring line-- to clearly that the "wiring line" and not the "circuit block" is formed in any layer of the semiconductor device.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the

United States and was published under Article 21(2) of such treaty in the English language.

8. **Claims 1-2,5** are rejected under 35 U.S.C. 102(e) as being anticipated by **Dahl** (US Patent No. 6,823,501).

As per **claims 1,5**, the elements of the claims are summarized in col. 2, lines 16-52, wherein planar-arrangement corresponds to the laying out of the bumps/bond pads, I/O cells, and edge logic cells in respective bumps/bond pads areas, I/O cells areas, and/or edge logic cell areas, wherein at least the edge logic cells correspond to the circuit blocks to be to arranged, wherein bumps/bond pads and/or I/O cells correspond to the terminals to be arranged, which include measurement terminals (i.e., JTAG terminals which are known in the art as terminals used for testing and/or measuring embedded integrated circuits) (see col. 17, lines 46-54; col. 15, lines 22-40); wherein the establishing the connect corresponds to the routing being performed (see col. 2, lines 45-48; col. 11, lines 47-67; col. 14, lines 1-19); wherein the terminal/pad having electrode formed in an uppermost layer of the semiconductor device is further described in col. 7, lines 32-41; and wherein since the terminals (i.e., I/O cells, pads, JTAG cells) as well as the circuit blocks (i.e., at least the edge logics) are treated as cells upon which the design rules are applied (see col. 11, lines 24-45 for spacing requirements; col. 14, lines 28-58 for timing requirement; col. 15, line 42 to col. 16, line 9, preliminary constraints that include the number of pins and signals needed for the layout), during the partitioning/floorplanning and routing steps, such registering step must necessarily takes place in order for the terminals (i.e., I/O cells, pads, JTAG cells) to be treated as cells, among the cells to be placed, upon which the design rules are

applied; wherein program for making the computer to execute the operation is further described in col. 5, line 24 to col. 6, line 18 (see Fig. 2) as part of the computer system upon which the method is implemented.

As per **claim 2**, all of the elements of claim 1, from which the claim depends, is discussed in the rejection of claim 1 above, wherein the further limitation in which the connection is performed based on the netlist stored is also described in col. 2, lines 34-39 (see also col. 11, line 51 to col. 12, line 63).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Application is requested herein to consider them carefully in response to this Office Action. In particular, the following prior arts made of record are most relevant:

Muranaka (U.S. Patent No. 6,941,536) discloses I/O cells placement and routing, which includes JTAG cells/terminals for testing/measuring of embedded integrated circuits (especially col. 44, line 57 to col. 45, line 65; abstract; Fig. 57);

Osaki et al. (U.S. Patent Application Publication No. 2002/0004929) discloses I/O cells, including test terminals, placement (abstract; paragraphs [0052]-[0054]);

Anzai (U.S. Patent Application Publication No. 2002/0004929) disclose I/O cells placement with test terminals arrangement (see especially abstract; paragraphs [0046]-0051]);

Alswede et al. (U.S. Patent No. 5,981,302) discloses terminals/pads arrangement at topmost layer of semiconductor device in accordance with the design rules (see especially abstract; col. 7, lines 10-26, 53-64; col. 8, lines 24-43);

Dervisoglu et al. (U.S. Patent No. 6,631,504) discloses hierarchical circuit placement, including the placement of scan circuits having test access port terminals (see especially col. 4, line 18 to col. 5, line 45).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 571-272-1895. The examiner can normally be reached on Monday-Thursday, 6:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

571-273-8300

Phallaka Kik
U.S. Patent Examiner
December 23, 2005